

# MML technology for film capacitors miniaturization

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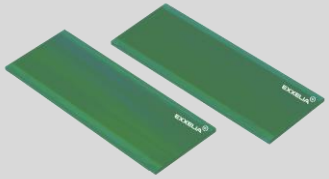
ESA/ESTEC, Noordwijk, The Netherlands

# Exxelia MML (Miniature Micro-Layer) Capacitors

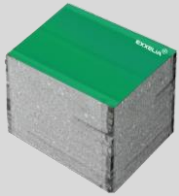
GLOBAL BUSINESS  
UNIT CAPACITORS



Similar to stacked capacitors, the MML are produced in a single step process :



The individual capacitors are stacked in parallel :



The packaging and leads allow to protect the capacitor and adapt it to the application:

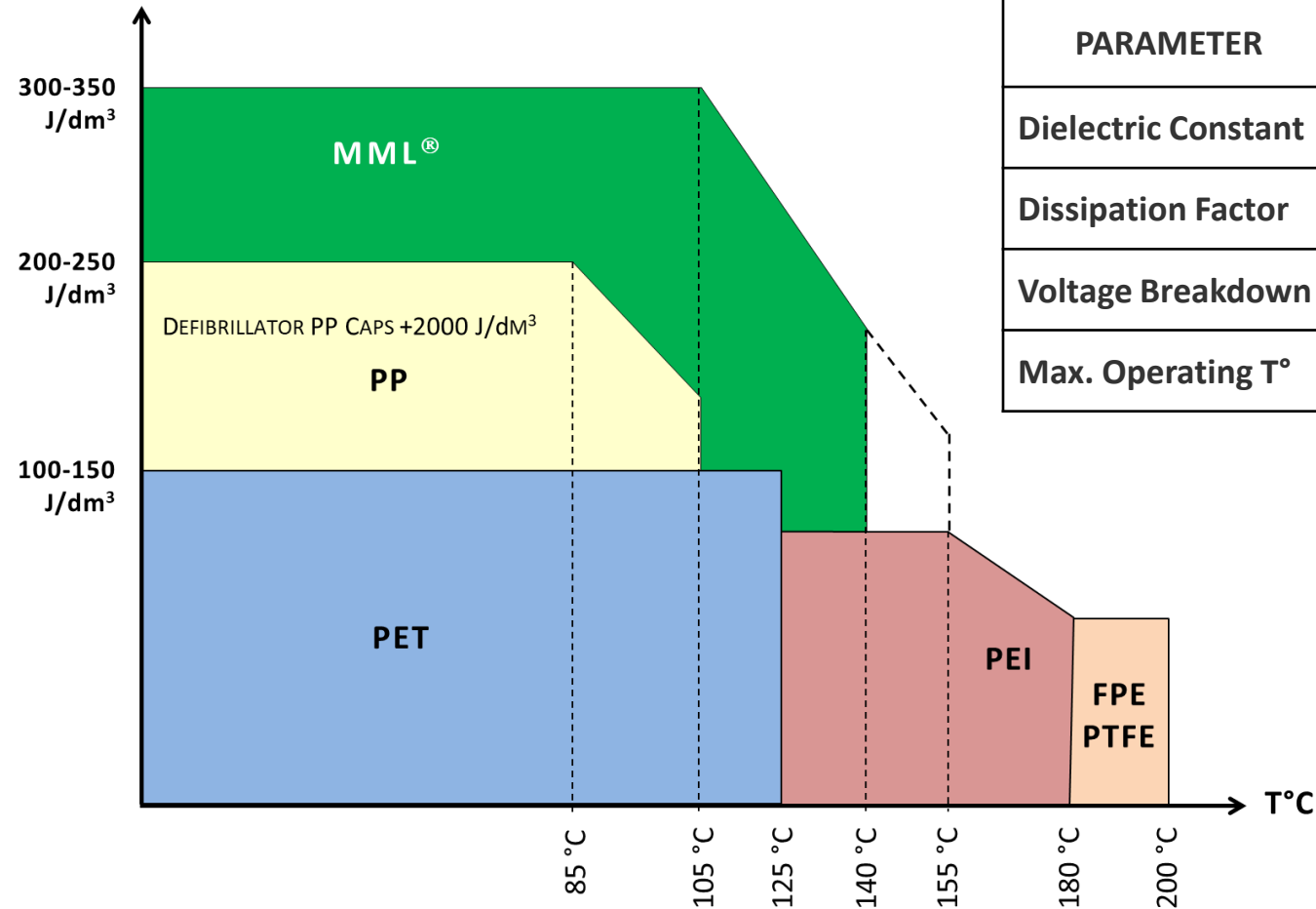


Miniaturization  $\Rightarrow$  Energy Density =  $\frac{E}{\text{Volume}}$

$$E = \frac{V^2 C}{2}$$

$$C = \frac{\epsilon S}{e}$$

Energy Density



| PARAMETER                  | MML                         | PP                        | PET                       |
|----------------------------|-----------------------------|---------------------------|---------------------------|
| <b>Dielectric Constant</b> | 3.2                         | 2.2                       | 3.3                       |
| <b>Dissipation Factor</b>  | $60 \cdot 10^{-4}$          | $2 \cdot 10^{-4}$         | $50 \cdot 10^{-4}$        |
| <b>Voltage Breakdown</b>   | $> 800\text{V}/\mu\text{m}$ | $700\text{V}/\mu\text{m}$ | $500\text{V}/\mu\text{m}$ |
| <b>Max. Operating T°</b>   | 140°C                       | 105°C                     | 125°C                     |

**Main MML advantages :**

- Miniaturization
- Higher temperature

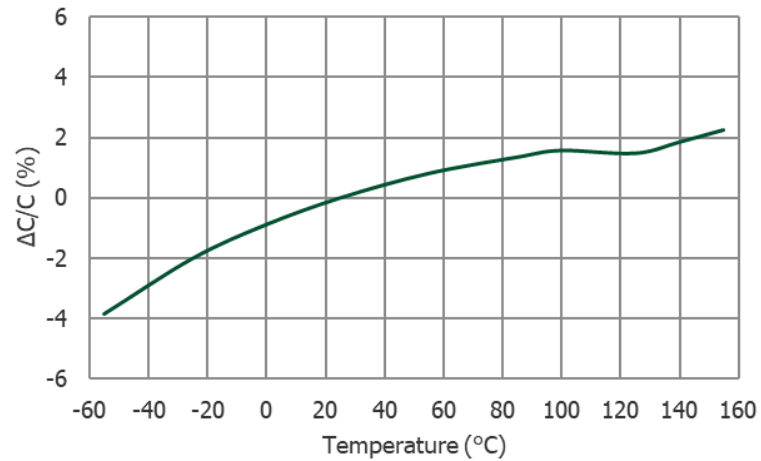
MML is well adapted  
for DC Filtering



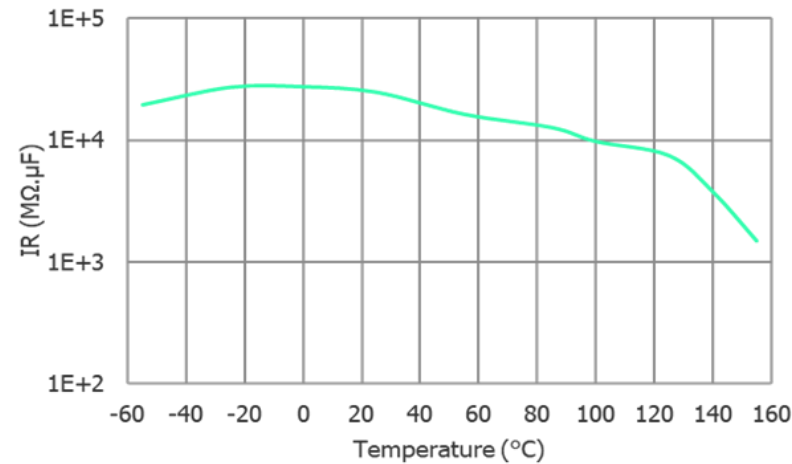
## Main Electrical Characteristics versus Temperature



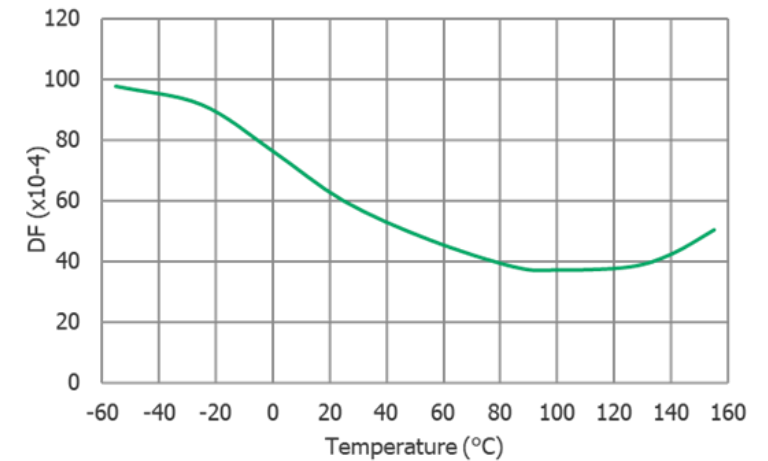
Capacitance drift vs temperature



Insulation Resistance vs temperature



Dissipation Factor vs temperature



- MML present a low capacitance drift for **DC filtering applications**
- There is no capacitance drift under voltage (as for other Film technologies)

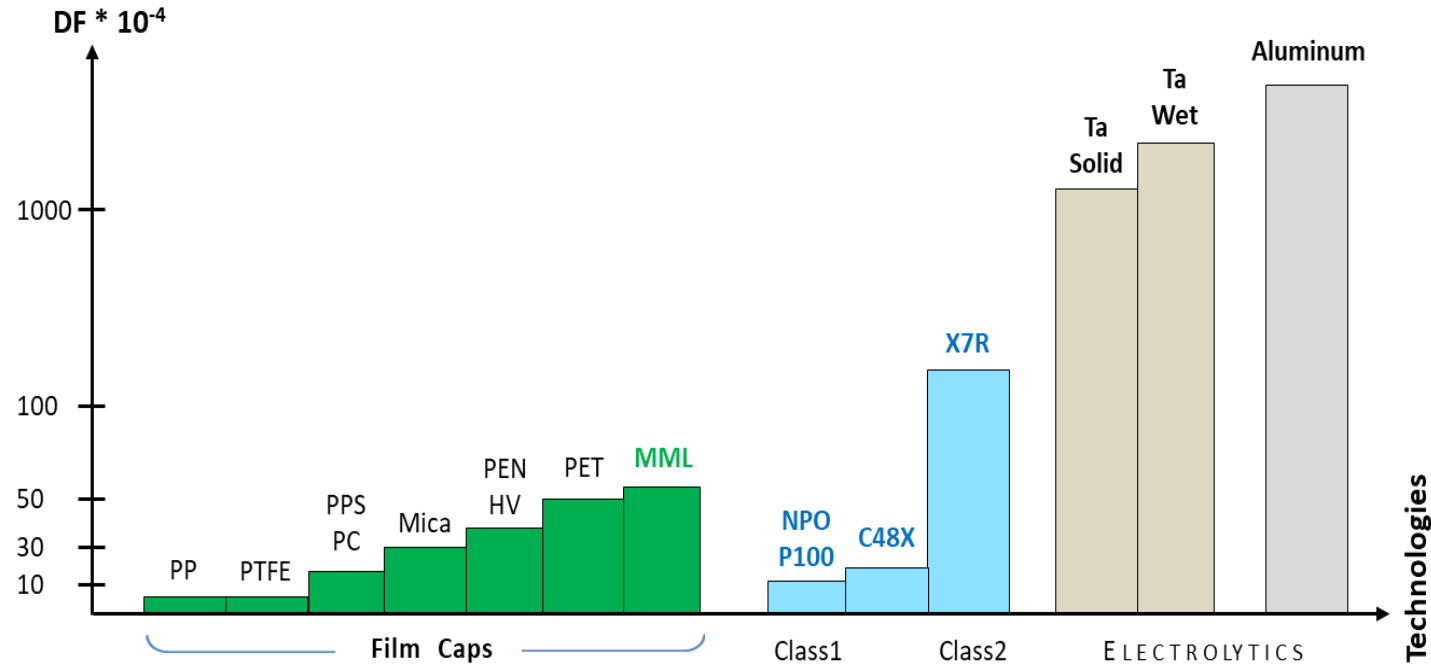
- Stable Insulation Resistance up to 125 $^{\circ}\text{C}$
- Decreasing of the IR upper 125 $^{\circ}\text{C}$  (increasing of the leakage current)
- Voltage derating between 125 $^{\circ}\text{C}$  / 140 $^{\circ}\text{C}$

Dissipation factor presents dielectric losses and **power behavior** of the technology

- Relatively low Dissipation Factor
- DF decreases for higher temperatures



## Dissipation Factor for Main Capacitor Technologies

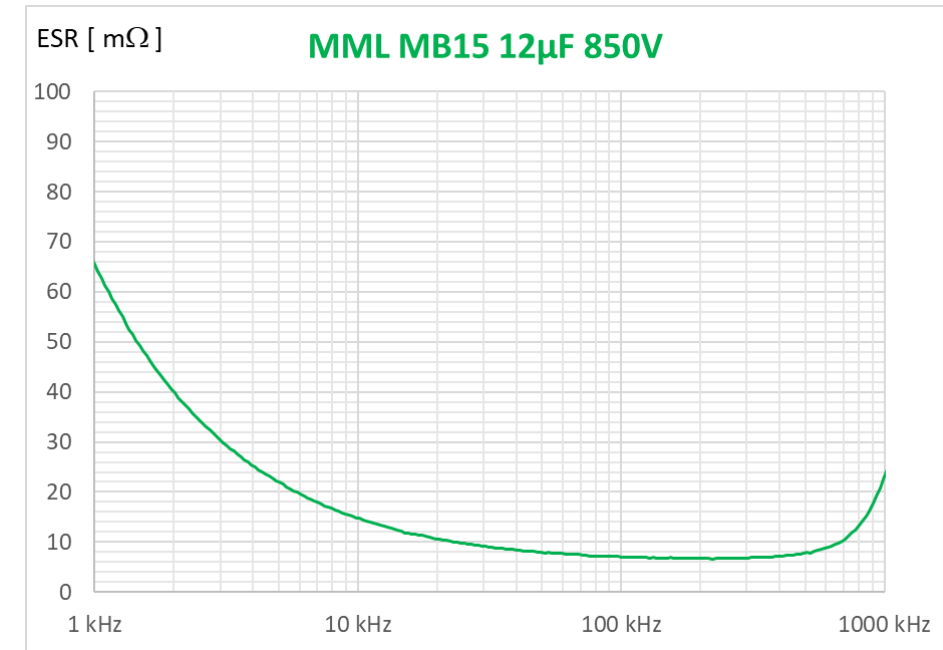


$$P_{\text{LOSSES}} = I_{\text{RMS}}^2 \cdot \text{ESR}$$

$$\text{ESR} = R_s + \frac{\text{DF}}{2\pi f C}$$

The DF, presenting dielectric losses, limits MML power behavior for low frequency AC filtering

- With comparison to other Film technologies, MML presents similar characteristics to Polyesters and is well adapted for DC filtering and energy storage
- MML technology has much lower dielectric losses compare to Ceramic capacitors and other technological families



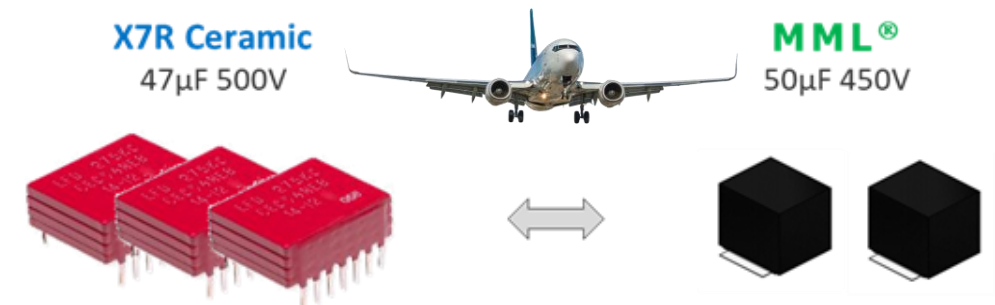
# MML miniaturization versus X7R ceramics



| TYPICAL CHARACTERISTICS |                     | FILM<br>MML <sup>®</sup>                                    | CERAMIC<br>X7R   |
|-------------------------|---------------------|---|--|
| RELIABILITY             | Self-Healing        | Excellent   | NO   |
|                         | Failure Mode        | Open Circuit  | Short-Circuit  |
| CAPACITANCE<br>DRIFT    | T° = -55°C / +125°C | -4% / <b>+2%</b> (typical)                                  | +15% / <b>-15%</b>   |
|                         | Under Rated Voltage | <b>No Drift</b>   | <b>-30% to -50%</b>  |
|                         | Operating Life      | ± 5%  | ± 12.5%  |
| POWER<br>BEHAVIORS      | DF (Tg d)           | < 100 . 10 <sup>-4</sup><br>(60 . 10 <sup>-4</sup> typical) | < 250 . 10 <sup>-4</sup><br>(150 . 10 <sup>-4</sup> typical) |
|                         | RMS Current         | Low ESR for HF  | Higher Dielectric Losses                                     |
|                         | Discharging         | High dV/dt & i <sup>2</sup> t                               | Fragile -> Cracks  |
| MASSE                   | for same Size       | Low ( ~ 4 times lower)                                      | Heavy  |
| ThermoMech.             | withstanding        | Flexible Structure  | Fragile, T° shock Sensitive                                  |
| CASING                  | type                | Case packaging needed                                       | <b>Chips available</b>                                       |
| Voltage Range           | Low voltages        | adapted for > 50V <sub>DC</sub>                             | <b>low voltage available</b>                                 |

Example of MML capability to replace  
some big stacked Ceramic capacitors

| Criteria                        | 1  | 2 | 3 | 1                     | 2 |
|---------------------------------|--|---|---|-----------------------|---|
|                                 | Ceramic X7R                                      |   |   | MML <sup>®</sup>      |   |
| Total Capacitance               | 3*47μF = 141μF                                   |   |   | 2 * 50 μF             |   |
| Total Cap requirement           | > 100 μF   |   |   | > 100 μF              |   |
| Operating temp                  | -55°C / 125°C                                    |   |   | -55°C / 140°C         |   |
| DF (typical) at 25°C            | 150 . 10 <sup>-4</sup>                           |   |   | 60 . 10 <sup>-4</sup> |   |
| Total Volume                    | 121 cm <sup>3</sup>                              |   |   | 40 cm <sup>3</sup>    |   |
| Energy Density<br>(after drift) | 145 J/dm <sup>3</sup><br>~ 100 J/dm <sup>3</sup> |   |   | 250 J/dm <sup>3</sup> |   |
| Total Weight                    | ~ 650 g  |   |   | ~ 65 g                |   |
| Failure Mode                    | Short Circuit                                    |   |   | Open Circuit          |   |





**ESA STANDARDS SYSTEM IS THE ONLY HAVING A REAL TECHNOLOGICAL APPROACH**



**EVALUATION** -> to demonstrate the technological limits, acceleration factors, EOL characteristics, failure mode, reliability level

**QUALIFICATION** -> to qualify Design / Product / Process -> demonstrate it periodically

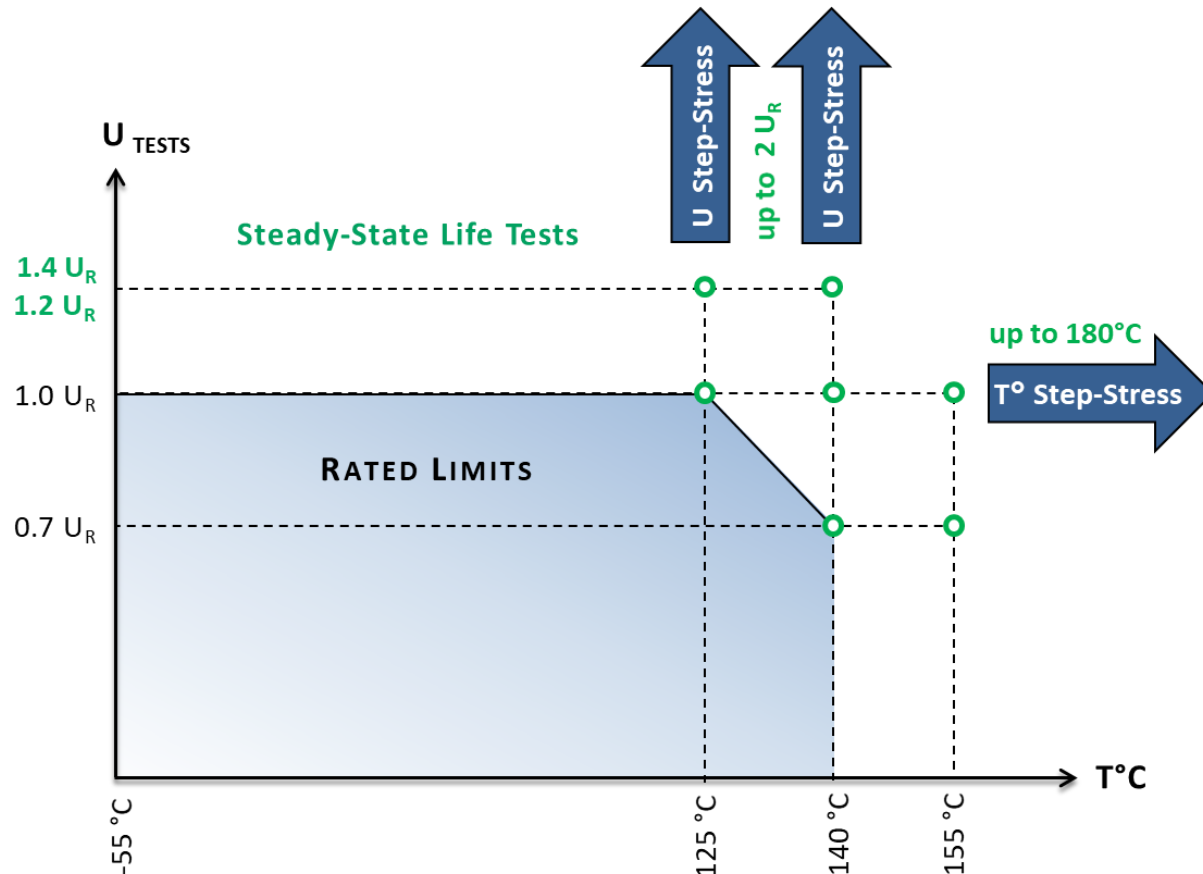
# MML Rated Limits and Evaluation Tests



MML capacitor testing with Technological Evaluation Approach

Goals : to define acceleration factors, EOL characteristics, demonstrate the open circuit failure mode, reliability level

Ongoing tests since 2019

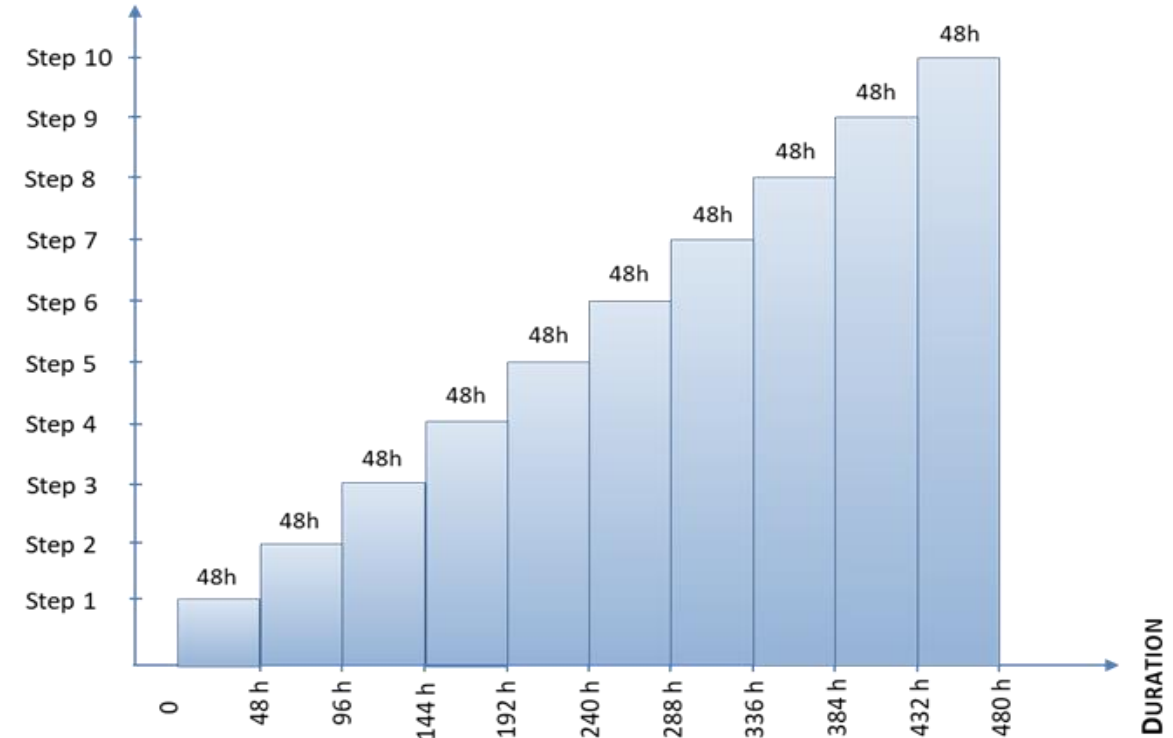


Voltage Step-Stress  
 $U_{n+1} = U_n + 0,2 \cdot U_{RC}$   
at constant temperature

Temperature Step-Stress  
 $T_{n+1} = T_n + 10^{\circ}C$   
under constant voltage

U and T°  
acceleration

## STEP-STRESS TESTS

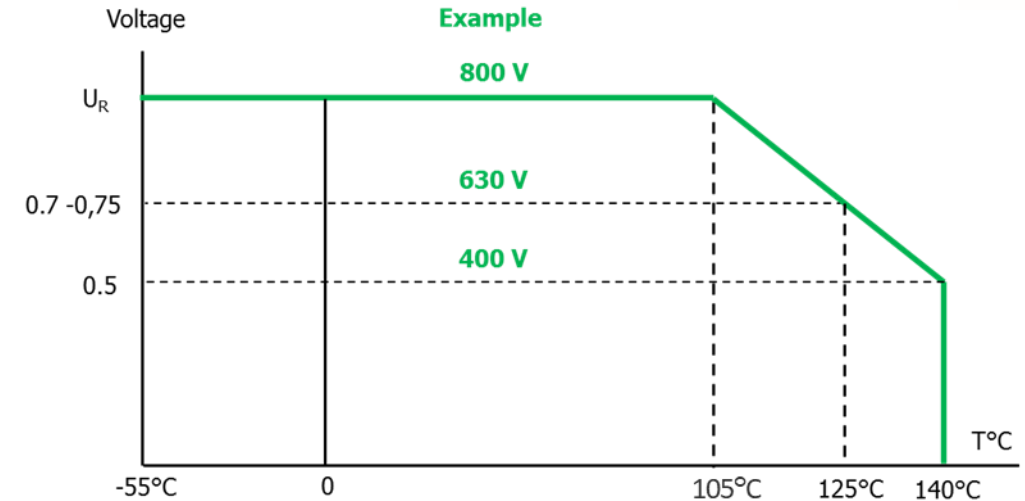


# MML Evaluation Tests – Example of Step-Stress testing



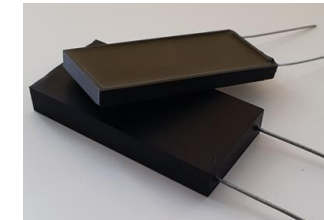
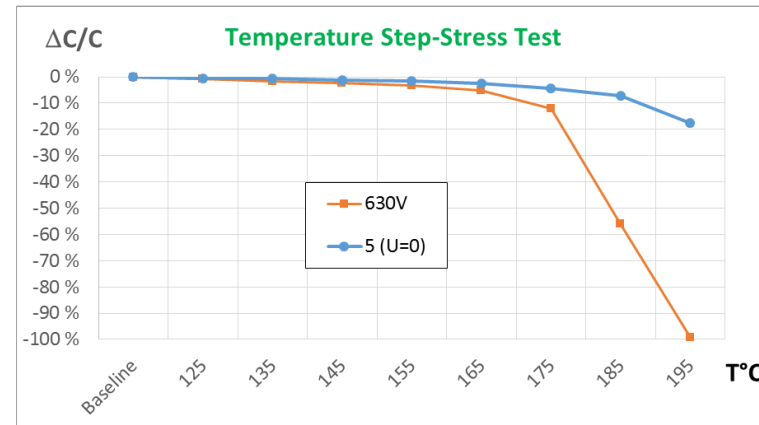
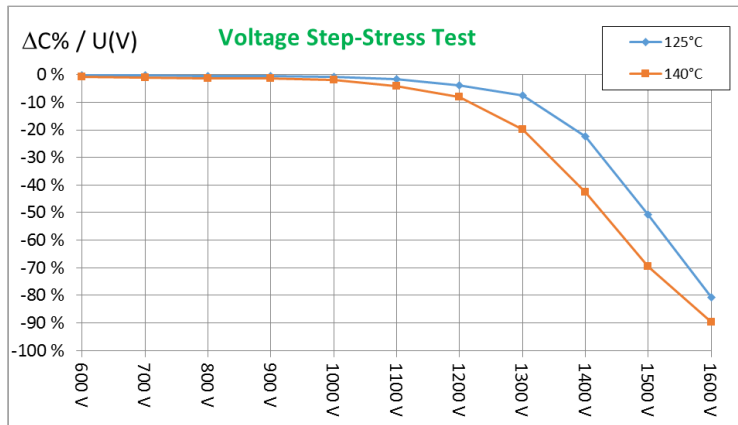
## MML cap Element

| Dimensions (mm)       |                         | L = 55    | W= 21,3  | H = 4 |
|-----------------------|-------------------------|-----------|----------|-------|
| C @ 1 kHz             | 7,25 $\mu$ F $\pm$ 10%  |           |          |       |
| U <sub>R</sub>        | 800 V <sub>DC</sub>     |           |          |       |
| Operating temperature | -55 °C / +140 °C        |           |          |       |
| DF @ 1 kHz            | $\leq 70 \cdot 10^{-4}$ |           |          |       |
| IR @ (500V- 1min)     | $\geq 2200$ M $\Omega$  |           |          |       |
| Dimensions*           | L = 60 mm               | W = 30 mm | H = 9 mm |       |



Voltage Step-Stress up to 2\*U<sub>R</sub> without any short-circuit failure thanks to selfhealing behavior (step 48h at 125°C and 140°C).

T° Step-Stress (step 48h under 630V) validated up to 180°C with stable characteristics and no short-circuit failure.

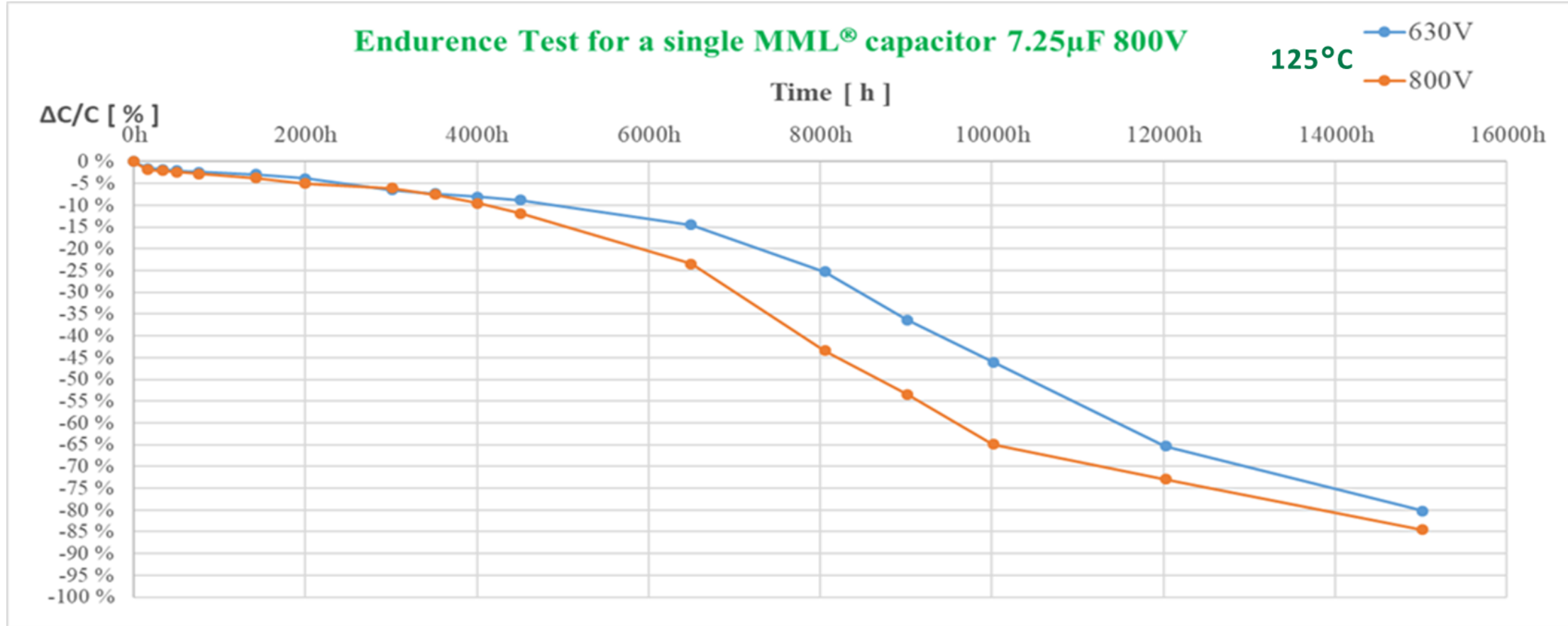






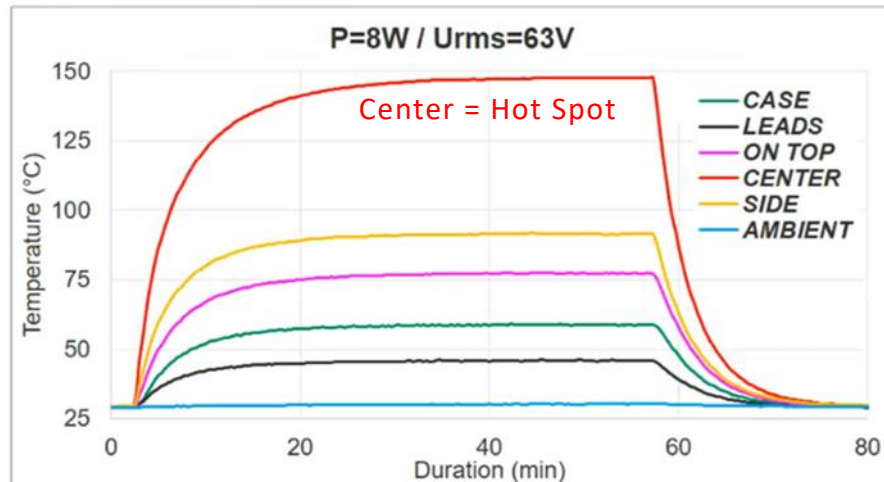
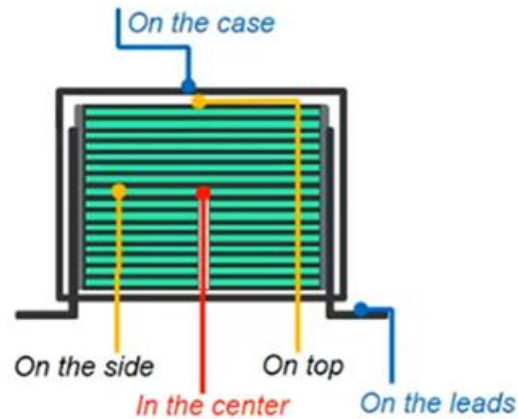
Example of MML capacitor long endurance testing at 125°C

More than 15 000 hours testing for Open-Circuit Failure Mode demonstration



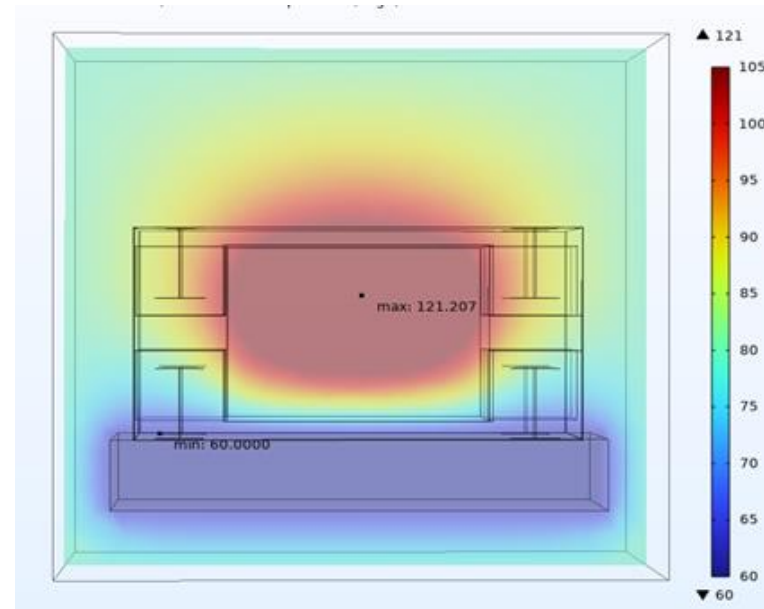


## Example of $R_{TH}$ evaluation



The size reduction of the MML capacitors has the consequence of decreasing the external surface needed for the thermal exchange.

For high-power filtering, a compromise must be made between size reduction and capacitance value in order to limit the ripple current and internal heating.



Multiscale modeling for a capacitor integrated on cooled base plate